Low Capacitance, 16- and 8-Channel ±15 V/+12 V *i*CMOS™ Multiplexers

ADG1206/ADG1207

FEATURES

<1 pC charge injection over full signal range
1.5 pF off capacitance
33 V supply range
120 Ω on resistance
Fully specified at ±15 V/+12 V
3 V logic-compatible inputs
Rail-to-rail operation
Break-before-make switching action
28-lead TSSOP and 32-lead, 5 mm × 5 mm LFCSP_VQ

APPLICATIONS

Audio and video routing
Automatic test equipment
Data acquisition systems
Battery-powered systems
Sample-and-hold systems
Communication systems

FUNCTIONAL BLOCK DIAGRAMS

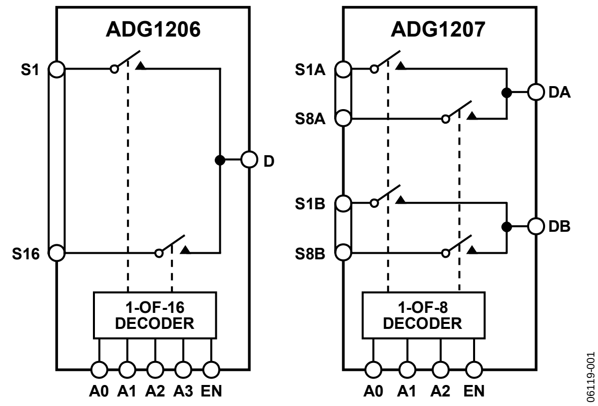

Figure 1.

GENERAL DESCRIPTION

The ADG1206 and ADG1207 are monolithic *i*CMOS analog multiplexers comprising sixteen single channels and eight differential channels, respectively. The ADG1206 switches one of sixteen inputs to a common output, as determined by the 4-bit binary address lines A0, A1, A2, and A3. The ADG1207 switches one of eight differential inputs to a common differential output, as determined by the 3-bit binary address lines A0, A1, and A2. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched off. When on, each channel conducts equally well in both directions and has an input signal range that extends to the supplies.

The *i*CMOS (industrial CMOS) modular manufacturing process combines high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and exceptionally low charge injection of these multiplexers make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Figure 2 shows that there is minimum charge injection over the entire signal range of the device. *i*CMOS construction also ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

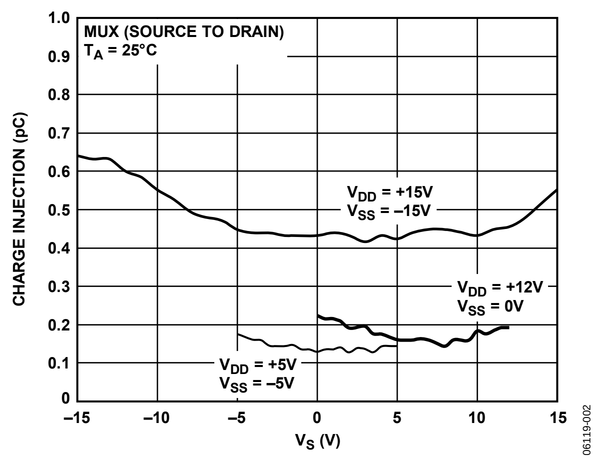

Figure 2. Source-to-Drain Charge Injection vs. Source Voltage

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REVISION HISTORY

7/06—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.[1]

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance, R_{ON}	120			Ω typ	V_S = ±10 V, I_S = −1 mA; see Figure 28
	200	240	270	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between Channels, ΔR_{ON}	3.5			Ω typ	V_S = ±10 V, I_S = −1 mA
	6	10	12	Ω max	
On Resistance Flatness, R_{FLAT} (On)	20			Ω typ	V_S = −5 V, 0 V, +5 V; I_S = −1 mA
	64	76	83	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	±0.03			nA typ	V_D = ±10 V, V_S = ∓10 V; see Figure 29
	±0.2	±0.6	±1	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = 1 V, 10 V; V_D = 10 V, 1 V; see Figure 29
	±0.2	±0.6	±2	nA max	
Channel On Leakage, I_D, I_S (On)	±0.08			nA typ	V_S = V_D = ±10 V; see Figure 30
	±0.2	±0.6	±2	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, $t_{TRANSITION}$	80			ns typ	R_L = 300 Ω, C_L = 35 pF
	130	165	185	ns max	V_S = 10 V; see Figure 31
t_{ON} (EN)	75			ns typ	R_L = 300 Ω, C_L = 35 pF
	95	105	115	ns max	V_S = 10 V; see Figure 33
t_{OFF} (EN)	85			ns typ	R_L = 300 Ω, C_L = 35 pF
	100	125	140	ns max	V_S = 10 V; see Figure 33
Break-Before-Make Time Delay, t_{BBM}	20			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 10 V; see Figure 32
Charge Injection	0.5			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 34
Off Isolation	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35
Channel-to-Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 37
Total Harmonic Distortion + Noise	0.15			% typ	R_L = 10 kΩ, 5 V rms, f = 20 Hz to 20 kHz; see Figure 38
−3 dB Bandwidth ADG1206	280			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 36
−3 dB Bandwidth ADG1207	490			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 36
C_S (Off)	1.5			pF typ	f = 1 MHz, V_S = 0 V
	2			pF max	f = 1 MHz, V_S = 0 V
C_D (Off) ADG1206	11			pF typ	f = 1 MHz, V_S = 0 V
	12			pF max	f = 1 MHz, V_S = 0 V
C_D (Off) ADG1207	7			pF typ	f = 1 MHz, V_S = 0 V
	9			pF max	f = 1 MHz, V_S = 0 V

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
C_D, C_S (On) ADG1206	13			pF typ	f = 1 MHz, V_S = 0 V
	15			pF max	f = 1 MHz, V_S = 0 V
C_D, C_S (On) ADG1207	8			pF typ	f = 1 MHz, V_S = 0 V
	10			pF max	f = 1 MHz, V_S = 0 V
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.002			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{DD}	260			μA typ	Digital inputs = 5 V
			420	μA max	
I_{SS}	0.002			μA typ	Digital inputs = 0 V, 5 V, or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			±5/±16.5	V min/max	GND = 0V

[1] Temperature range for Y version is −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.[1]

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance, R_{ON}	300			Ω typ	V_S = 0 V to10 V, I_S = −1 mA; see Figure 28
	475	567	625	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels, ΔR_{ON}	5			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	16	26	27	Ω max	
On Resistance Flatness, R_{FLAT} (On)	60			Ω typ	V_S = 3 V, 6 V, 9 V; I_S = −1 mA
LEAKAGE CURRENTS					V_{DD} = 13.2 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 29
	±0.2	±0.6	±1	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 29
	±0.2	±0.6	±2	nA max	
Channel On Leakage, I_D, I_S (On)	±0.08			nA typ	V_S = V_D = 1 V or 10 V; see Figure 30
	±0.2	±0.6	±2	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.001			μA typ	
			±0.1	μA max	V_{IN} = V_{INL} or V_{INH}
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, $t_{TRANSITION}$	100			ns typ	R_L = 300 Ω, C_L = 35 pF
	140	175	200	ns max	V_S = 8 V; see Figure 31
t_{ON} (EN)	80			ns typ	R_L = 300 Ω, C_L = 35 pF
	100	120	130	ns max	V_S = 8 V; see Figure 33
t_{OFF} (EN)	90			ns typ	R_L = 300 Ω, C_L = 35 pF
	110	130	155	ns max	V_S = 8 V; see Figure 33
Break-Before-Make Time Delay, t_{BBM}	25			ns typ	R_L = 300 Ω, C_L = 35 pF
			15	ns min	V_{S1} = V_{S2} = 8 V; see Figure 32
Charge Injection	0.2			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 34
Off Isolation	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 35
Channel-to-Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 37
−3 dB Bandwidth ADG1206	185			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 36
−3 dB Bandwidth ADG1207	300			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 36
C_S (Off)	1.5			pF typ	f = 1 MHz, V_S = 6 V
	2			pF max	f = 1 MHz, V_S = 6 V
C_D (Off) ADG1206	13			pF typ	f = 1 MHz, V_S = 6 V
	15			pF max	f = 1 MHz, V_S = 6 V
C_D (Off) ADG1207	9			pF typ	f = 1 MHz, V_S = 6 V
	11			pF max	f = 1 MHz, V_S = 6 V
C_D, C_S (On) ADG1206	15			pF typ	f = 1 MHz, V_S = 6 V
	17			pF max	f = 1 MHz, V_S = 6 V
C_D, C_S (On) ADG1207	10			pF typ	f = 1 MHz, V_S = 6 V
	12			pF max	f = 1 MHz, V_S = 6 V

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.002			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{DD}	260			µA typ	Digital inputs = 5
			420	µA max	
V_{DD}			5/16.5	V min/max	V_{SS} = 0 V, GND = 0 V

[1] Temperature range for Y version is −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog, Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	100 mA
Operating Temperature Ranges	
Industrial (Y Version)	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
28-Lead TSSOP	
θ_{JA}, Thermal Impedance	97.9°C/W
θ_{JC}, Thermal Impedance	14°C/W
32-Lead LFCSP_VQ	
θ_{JA}, Thermal Impedance	27.27°C/W
Reflow Soldering Peak Temperature (Pb-Free)	260(+0/−5)°C

[1] Overvoltages at A, EN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

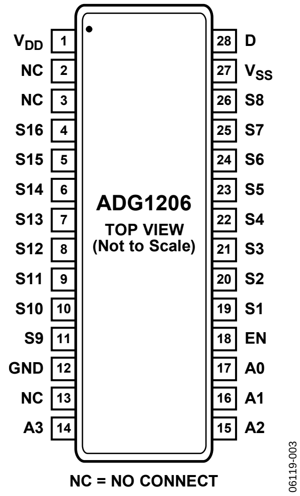

Figure 3. ADG1206 Pin Configuration—TSSOP

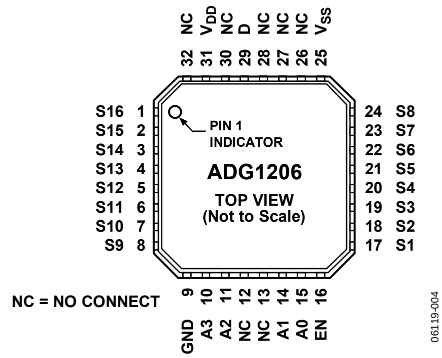

Figure 4. ADG1206 Pin Configuration—5 mm × 5 mm LFCSP_VQ, Exposed Pad Tied to Substrate, V_{SS}

Table 4. ADG1206 Pin Function Descriptions

Pin Number			
TSSOP	**LFCSP_VQ**	**Mnemonic**	**Description**
1	31	V_{DD}	Most Positive Power Supply Potential.
2	12, 13	NC	No Connect.
3	26, 27, 28, 30, 32	NC	No Connect.
4	1	S16	Source Terminal 16. Can be an input or an output.
5	2	S15	Source Terminal 15. Can be an input or an output.
6	3	S14	Source Terminal 14. Can be an input or an output.
7	4	S13	Source Terminal 13. Can be an input or an output.
8	5	S12	Source Terminal 12. Can be an input or an output.
9	6	S11	Source Terminal 11. Can be an input or an output.
10	7	S10	Source Terminal 10. Can be an input or an output.
11	8	S9	Source Terminal 9. Can be an input or an output.
12	9	GND	Ground (0 V) Reference.
13	–	NC	No Connect.
14	10	A3	Logic Control Input.
15	11	A2	Logic Control Input.
16	14	A1	Logic Control Input.
17	15	A0	Logic Control Input.
18	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19	17	S1	Source Terminal 1. Can be an input or an output.
20	18	S2	Source Terminal 2. Can be an input or an output.
21	19	S3	Source Terminal 3. Can be an input or an output.
22	20	S4	Source Terminal 4. Can be an input or an output.
23	21	S5	Source Terminal 5. Can be an input or an output.
24	22	S6	Source Terminal 6. Can be an input or an output.
25	23	S7	Source Terminal 7. Can be an input or an output.
26	24	S8	Source Terminal 8. Can be an input or an output.
27	25	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	29	D	Drain Terminal. Can be an input or an output.

Table 5. ADG1206 Truth Table

A3	A2	A1	A0	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

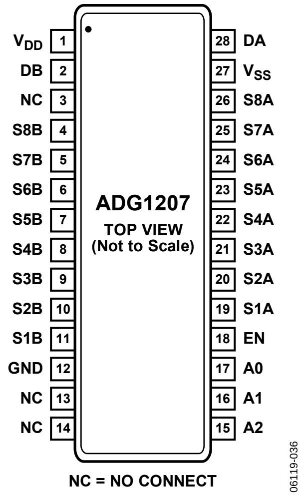

Figure 5. ADG1207 Pin Configuration—TSSOP

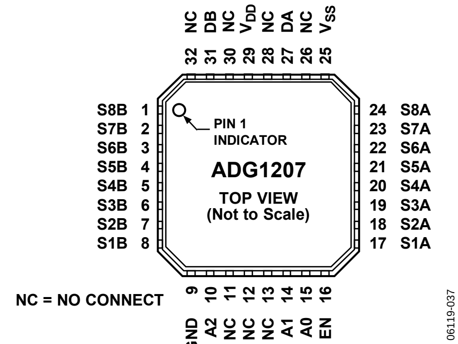

Figure 6. ADG1207 Pin Configuration—5 mm × 5 mm LFCSP_VQ Exposed Pad Tied to Substrate, V_{SS}

Table 6. ADG1207 Pin Function Descriptions

Pin Number			
TSSOP	**LFCSP_VQ**	**Mnemonic**	**Description**
1	29	V_{DD}	Most Positive Power Supply Potential.
2	31	DB	Drain Terminal B. Can be an input or an output.
3	11, 12, 13	NC	No Connect.
4	1	S8B	Source Terminal 8B. Can be an input or an output.
5	2	S7B	Source Terminal 7B. Can be an input or an output.
6	3	S6B	Source Terminal 6B. Can be an input or an output.
7	4	S5B	Source Terminal 5B. Can be an input or an output.
8	5	S4B	Source Terminal 4B. Can be an input or an output.
9	6	S3B	Source Terminal 3B. Can be an input or an output.
10	7	S2B	Source Terminal 2B. Can be an input or an output.
11	8	S1B	Source Terminal 1B. Can be an input or an output.
12	9	GND	Ground (0 V) Reference.
13	26, 28, 30, 32	NC	No Connect.
14	–	NC	No Connect.
15	10	A2	Logic Control Input.
16	14	A1	Logic Control Input.
17	15	A0	Logic Control Input.
18	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19	17	S1A	Source Terminal 1A. Can be an input or an output.
20	18	S2A	Source Terminal 2A. Can be an input or an output.
21	19	S3A	Source Terminal 3A. Can be an input or an output.
22	20	S4A	Source Terminal 4A. Can be an input or an output.
23	21	S5A	Source Terminal 5A. Can be an input or an output.
24	22	S6A	Source Terminal 6A. Can be an input or an output.
25	23	S7A	Source Terminal 7A. Can be an input or an output.
26	24	S8A	Source Terminal 8A. Can be an input or an output.
27	25	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	27	DA	Drain Terminal A. Can be an input or an output.

Table 7. ADG1207 Truth Table

A2	A1	A0	EN	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TYPICAL PERFORMANCE CHARACTERISTICS

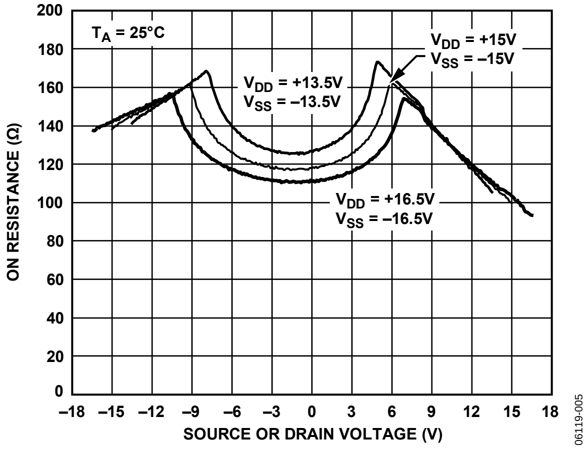

Figure 7. On Resistance as a Function of V_D (V_S) for Dual Supply

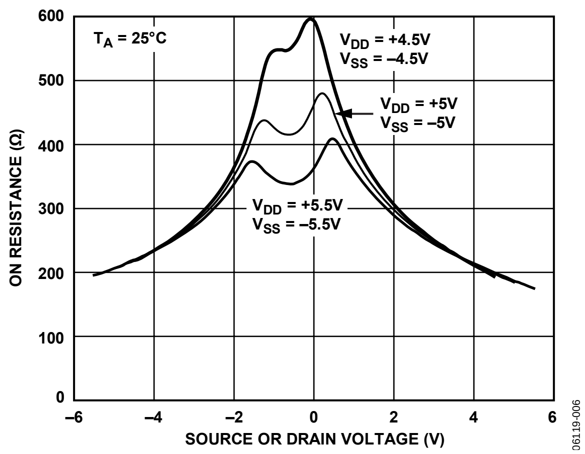

Figure 8. On Resistance as a Function of V_D (V_S) for Dual Supply

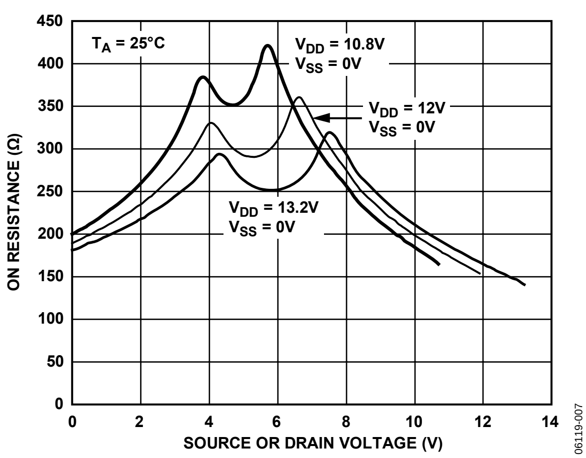

Figure 9. On Resistance as a Function of V_D (V_S) for Single Supply

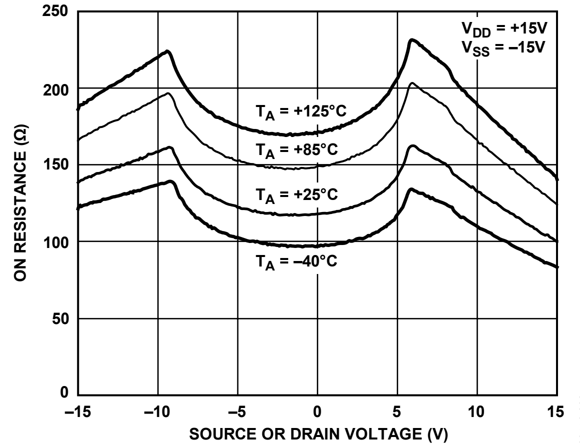

Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

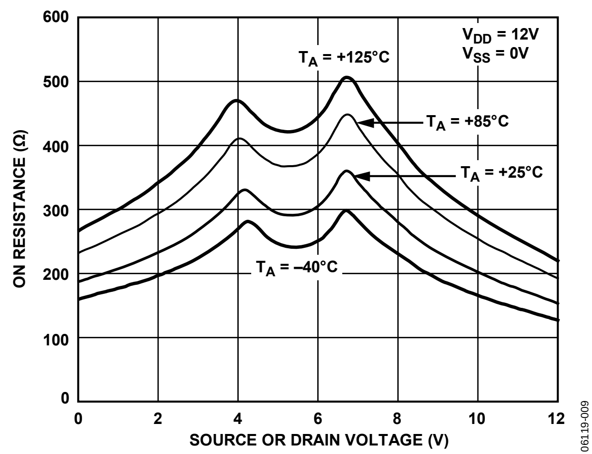

Figure 11. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

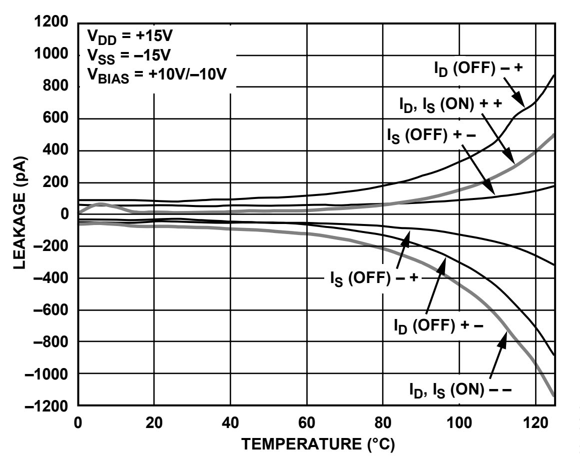

Figure 12. ADG1206 Leakage Currents as a Function of Temperature, Dual Supply

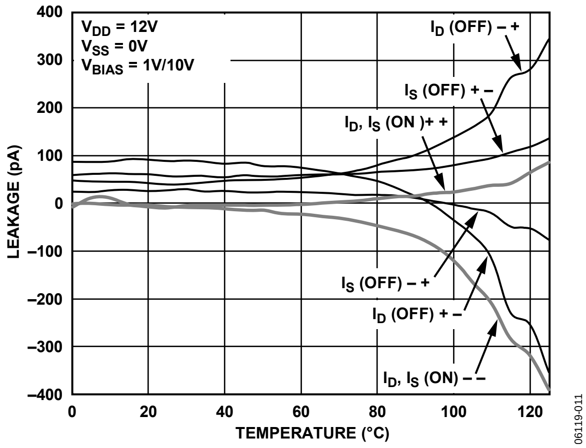

Figure 13. ADG1206 Leakage Currents as a Function of Temperature, Single Supply

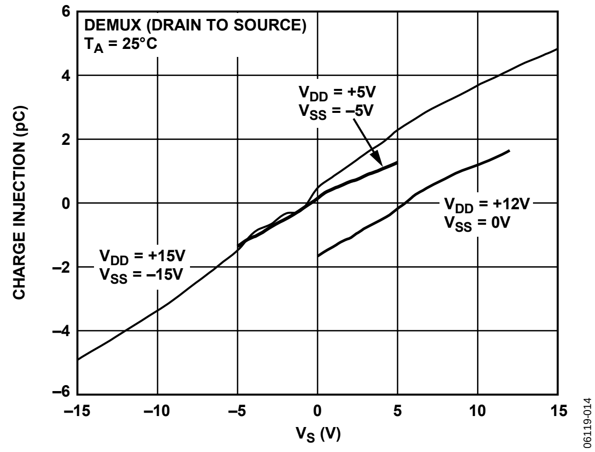

Figure 16. Drain-to-Source Charge Injection vs. Source Voltage

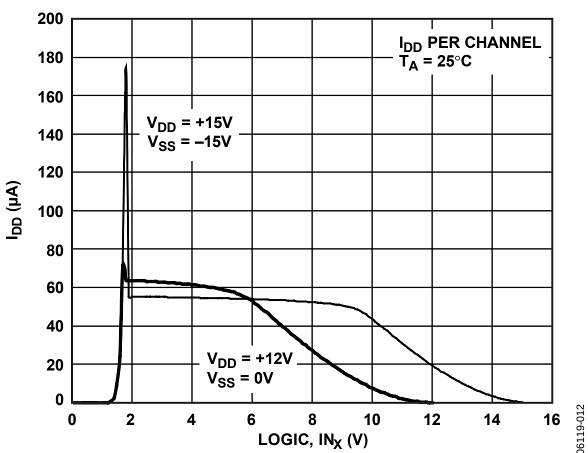

Figure 14. I_{DD} vs. Logic Level

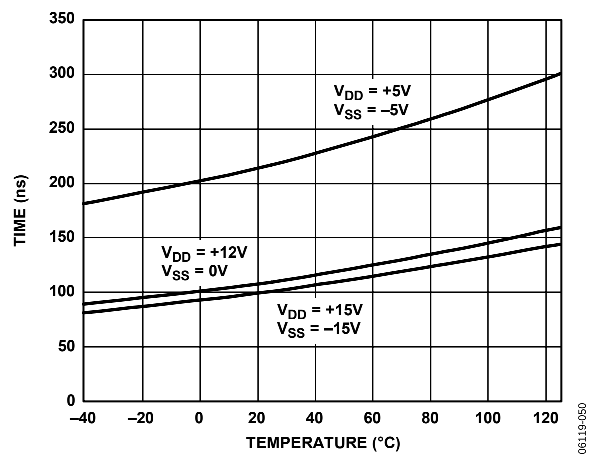

Figure 17. Transition Time vs. Temperature

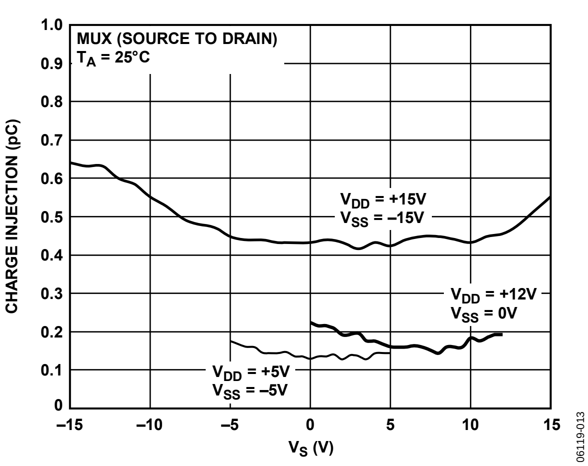

Figure 15. Source-to-Drain Charge Injection vs. Source Voltage

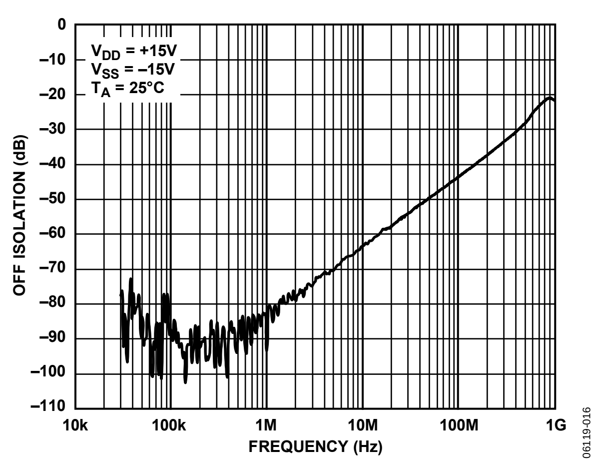

Figure 18. Off Isolation vs. Frequency

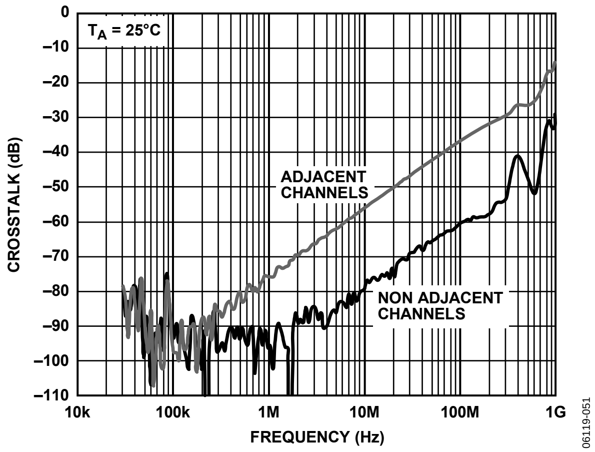

Figure 19. ADG1206 Crosstalk vs. Frequency

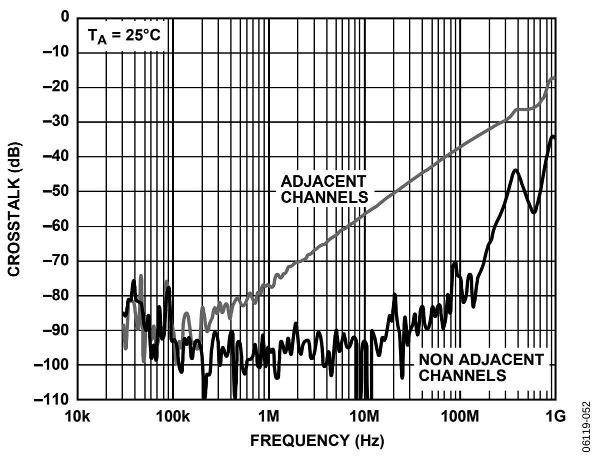

Figure 20. ADG1207 Crosstalk vs. Frequency

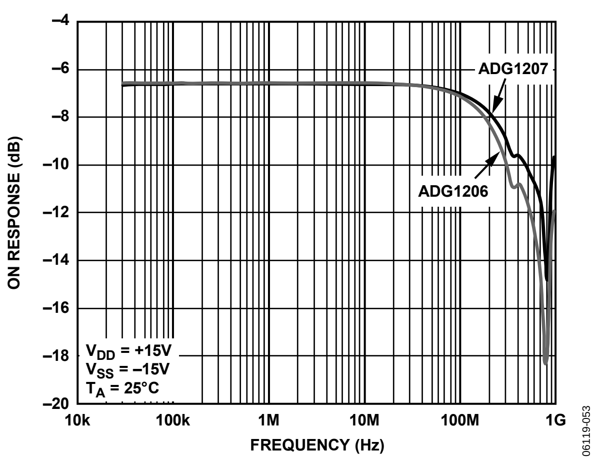

Figure 21. On Response vs. Frequency

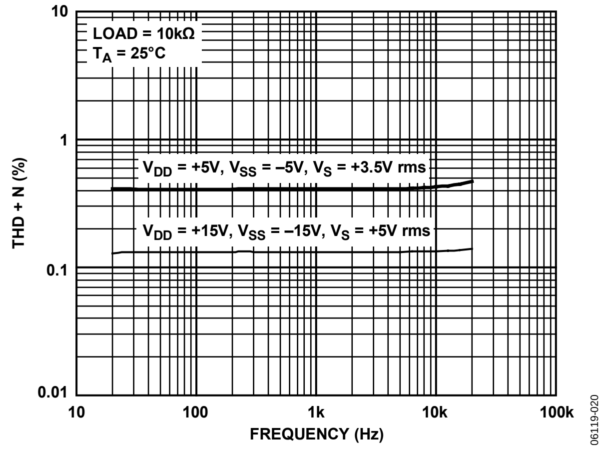

Figure 22. THD + N vs. Frequency

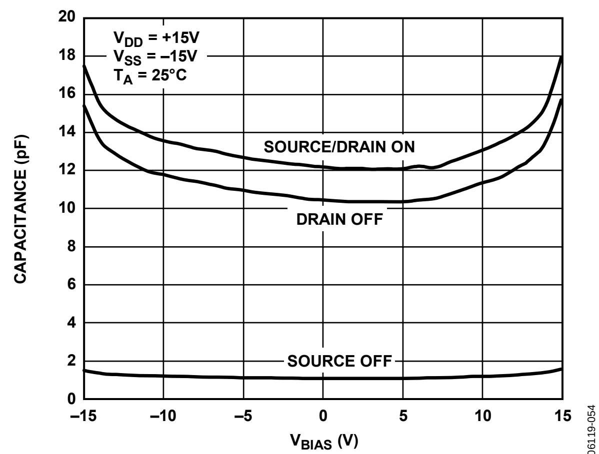

Figure 23. ADG1206 Capacitance vs. Source Voltage, ±15 V Dual Supply

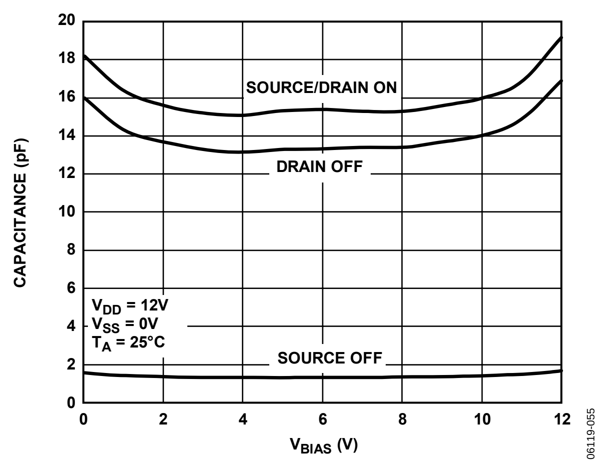

Figure 24. ADG1206 Capacitance vs. Source Voltage, 12 V Single Supply

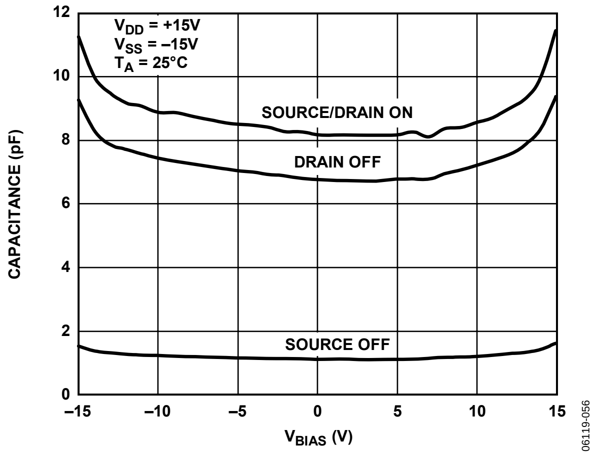

Figure 25. ADG1207 Capacitance vs. Source Voltage, ±15 V Dual Supply

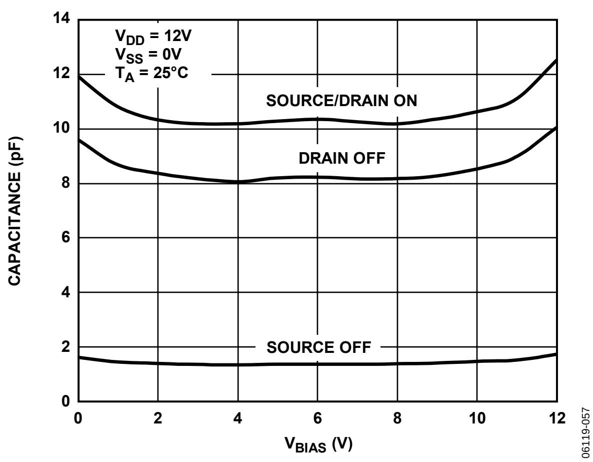

Figure 26. ADG1207 Capacitance vs. Source Voltage, 12 V Single Supply

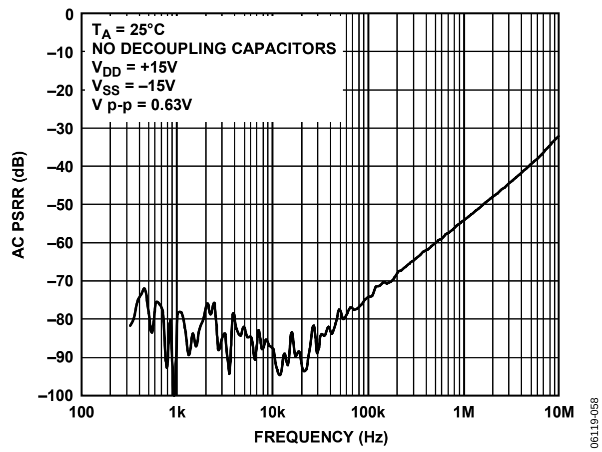

Figure 27. AC PSRR vs. Frequency

TERMINOLOGY

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
Difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

I_S (Off)
Source leakage current when the switch is off.

I_D (Off)
Drain leakage current when the switch is off.

I_D, I_S (On)
Channel leakage current when the switch is on.

V_D (V_S)
Analog voltage on Terminals D and S.

C_S (Off)
Channel input capacitance for the off condition.

C_D (Off)
Channel output capacitance for the off condition.

C_D, C_S (On)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} (EN)

Delay time between the 50% and 90% points of the digital input and the switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and the switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

T_{BBM}
Off time measured between the 80% points of the switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

ACPSRR (AC Power Supply Rejection Ratio)
Measures the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

TEST CIRCUITS

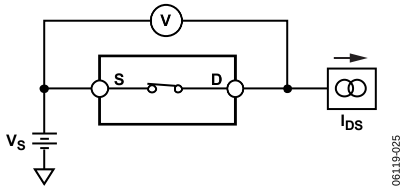

Figure 28. On Resistance

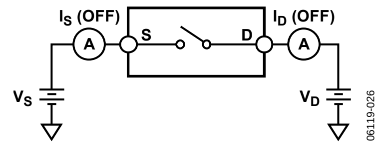

Figure 29. Off Leakage

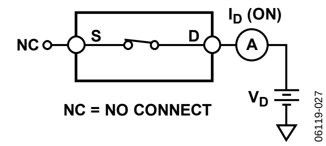

Figure 30. On Leakage

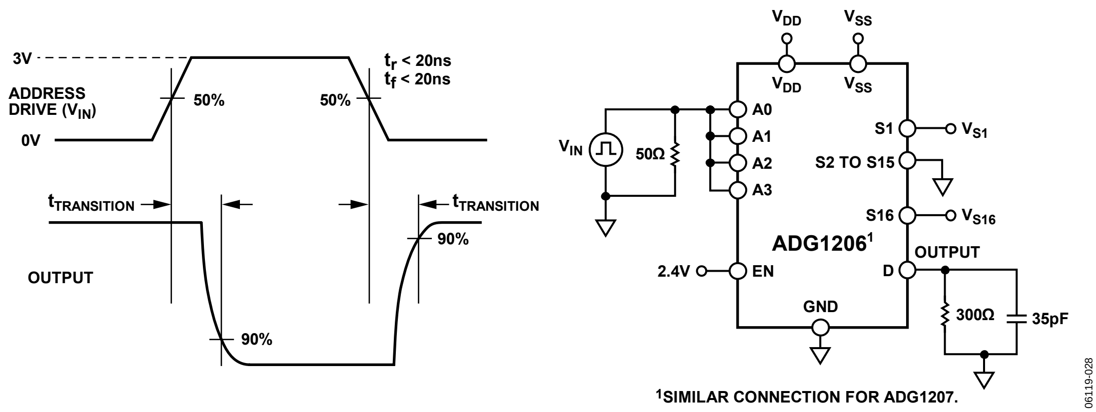

Figure 31. Address to Output Switching Times, $t_{TRANSITION}$

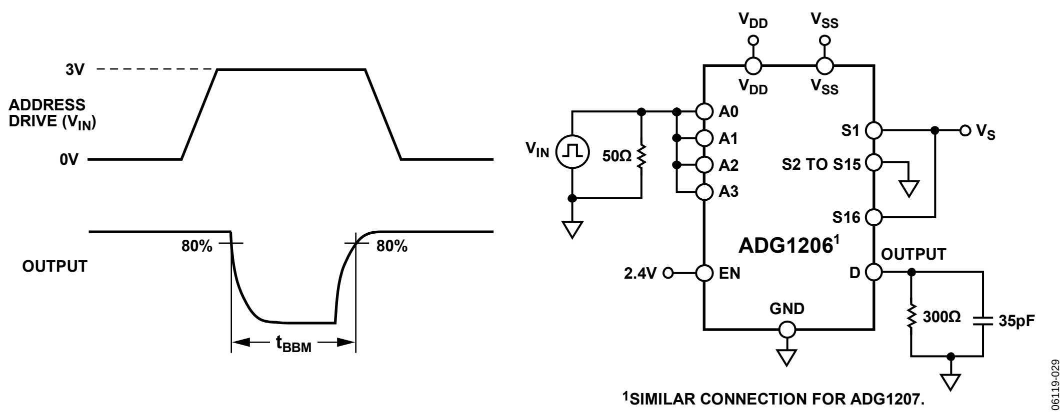

Figure 32. Break-Before-Make Delay, t_{BBM}

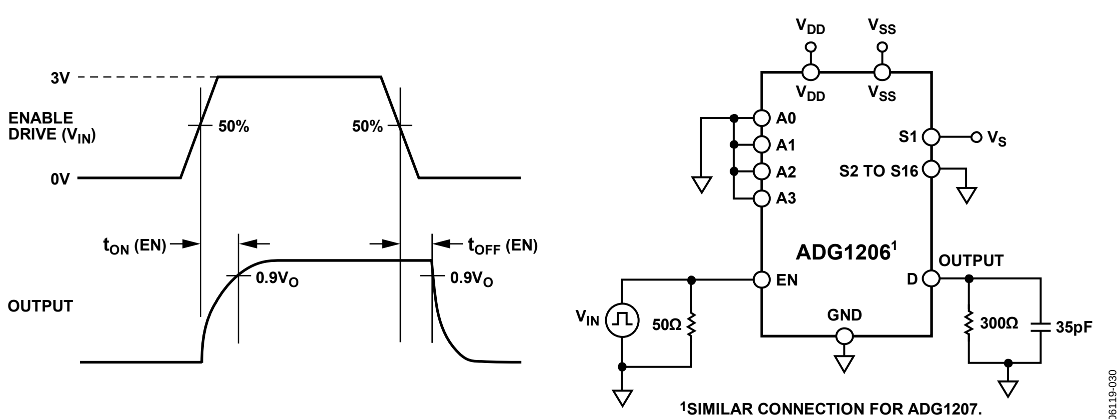

Figure 33. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

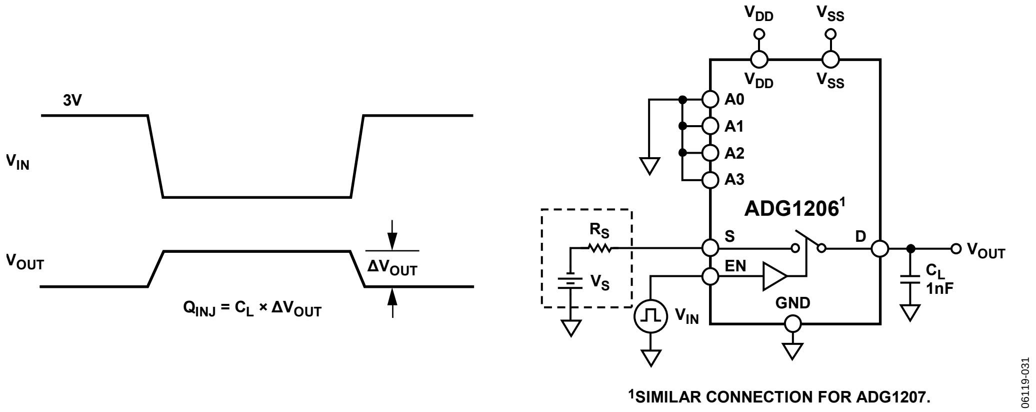

Figure 34. Charge Injection

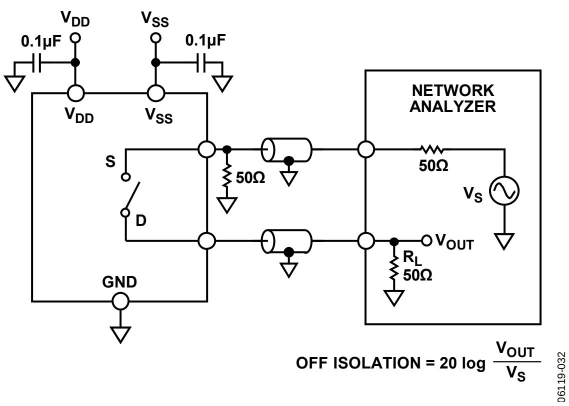

Figure 35. Off Isolation

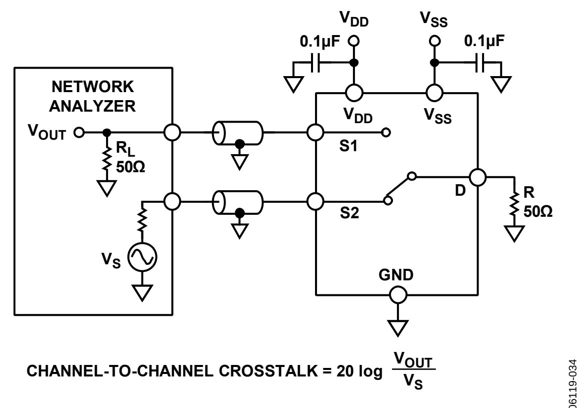

Figure 37. Channel-to-Channel Crosstalk

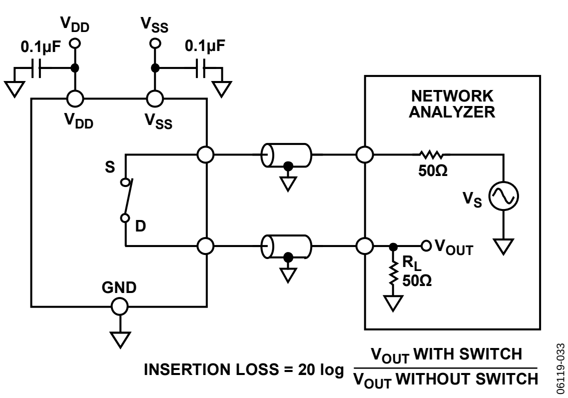

Figure 36. Bandwidth

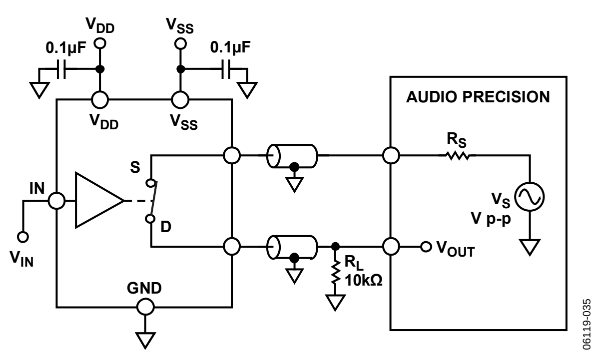

Figure 38. THD + Noise

OUTLINE DIMENSIONS

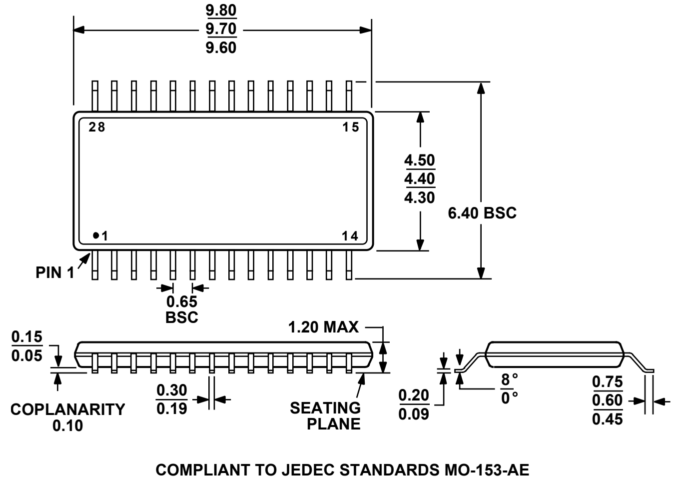

Figure 39. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters

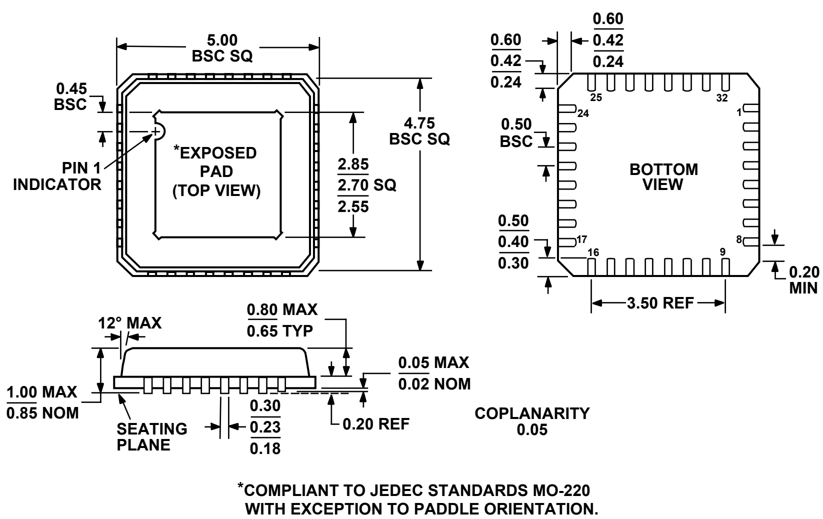

Figure 40. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Description	Package Option
ADG1206YRUZ[1]	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG1206YRUZ-REEL7[1]	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG1206YCPZ-REEL7[1]	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
ADG1207YRUZ[1]	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG1207YRUZ-REEL7[1]	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG1207YCPZ-REEL7[1]	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2

[1] Z = Pb-free part.

NOTES